CLAIMS

1. An arrangement comprising:

a source operative, between a first and a second DC terminal, to provide a DC voltage of substantially constant magnitude;

an inverter circuit connected with the DC terminals and functional to provide a high-frequency AC voltage between a reference terminal and an inverter output terminal; the high-frequency AC voltage being of a certain magnitude and a certain frequency; the certain frequency being substantially higher than the frequency of the power line voltage on an ordinary electric utility power line; the inverter circuit including a tuned L-C circuit connected in circuit with the inverter output terminal and the reference terminal; the L-C circuit having a tank capacitor parallel-connected with a tank inductor and being resonant at or near said certain frequency; any AC voltage of frequency equal to that of the high-frequency AC voltage that might exist between the inverter terminal and the first DC terminal being of negligible magnitude compared with said certain magnitude; any AC voltage of frequency equal to that of the high-frequency AC voltage that might exist between the first and second DC terminals being of magnitude negligible in comparison with said certain magnitude; and

gas discharge lamp means connected in circuit with the L-C circuit.

2. The arrangement of claim 1 wherein the gas discharge lamp means includes a gas discharge lamp series-connected with a current-limiting reactance means.

3. The arrangement of claim 1 wherein the high-frequency AC voltage is of substantially sinusoidal waveform.

4. The arrangement of claim 1 where the inverter circuit is characterized by including a first and a second transistor; the first transistor having a first transistor terminal; the second transistor having a second transistor terminal; the first transistor terminal being conected to the second transistor terminal; both transistor terminals being connected in circuit with the inverter output terminal in such manner that any voltage present between the inverter output terminal and either one of the two transistor terminals is of negligible magnitude compared with said certain magnitude.

5. The arrangement of claim 1 wherein the inverter circuit includes a first transistor having a first transistor terminal connected with the inverter output terminal in such manner that any voltage existing between the inverter output terminal and the first transistor terminal is of magnitude negligible compared with said certain magnitude; there being substantially zero resistance to the flow of unidirectional current between the inverter output terminal and the first transistor terminal.

6. An arrangement comprising:

a DC source functional to provide a DC supply voltage between a first and a second DC supply terminal;

an inverter circuit connected between the first and second DC supply terminals; the inverter circuit being functional to supply a high-frequency substantially sinusoidal AC output voltage between a first and a second AC output terminal; the high-frequency AC output voltage having a certain magnitude and being of frequecy substantially higher than that of the power line voltage on an ordinary electric utility power line; any high-frequency AC voltage that might exist between the second AC output terminal and one of the DC supply terminals being of negligible magnitude compared with said certain magnitude; the inverter circuit being further characterized by including: (i) a first transistor having a first control input terminal, a first output terminal, and a first common terminal; and (ii) a second transistor having a second control input terminal, a second output terminal, and a second common terminal; the second output terminal being connected with the first common terminal, thereby to form a junction terminal; the junction terminal being connected with the first AC output terminal in such manner that: (i) substantially no unidirectional voltage drop can exist between the junction terminal and the first AC output terminal, and (ii) any alternating voltage that might exist between the junction terminal and the first AC output terminal would be of negligible magnitude compared with said certain magnitude; a unidirectional voltage existing between the second common terminal and the first output terminal; the average magnitude of the unidirectional magnitude being substantially equal to that of the DC supply voltage; and

a gas discharge lamp connected in circuit with the AC output terminals.

7. The arrangement of claim 6 wherein the inverter circuit is characterized by being connected with the DC supply terminals by way of an inductor means.

8. An arrangement comprising:

an AC source functional to supply an AC power line voltage at a pair of AC power line terminals;

rectifying and filtering means connected with the AC power line terminals and functional to provide a DC supply voltage at a pair of DC supply terminals;

a gas discharge lamp having lamp terminals; and

an inverter-type ballasting circuit having DC input terminals connected with the DC supply terminals and AC output terminals connected with the lamp terminals; the inverter-type ballasting circuit being functional to power the gas discharge lamp and is otherwise characterized by: (i) having a first transistor with a first transistor terminal connected with a second transistor terminal of a second transistor; (ii) causing a substantially sinusoidal AC voltage to exist between the first transistor terminal and one of the DC input terminals; the frequency of the substantially sinusoidal AC voltage being substantially higher than that of the AC power line voltage.

9. The arrangement of claim 8 wherein a parallel-tuned L-C circuit is connected in circuit between the first transistor terminal and one of the DC input terminals; the parallel-tuned L-C circuit being naturally resonant at or near the fundamental frequency of the substantially sinusoidal AC voltage.

10. The arrangement of claim 8 wherein the absolute magnitude of the DC supply voltage is larger than the absolute peak magnitude of the AC power line voltage.

11. The arrangement of claim 8 wherein: (i) the first transistor has a first control input terminal, a first output terminal, and a first common terminal; (ii) the second transistor has a second control input terminal, a second output terminal, and a second common terminal; (iii) the first transistor terminal is the first transistor's common terminal; (iv) the second transistor terminal is the second transistor's output terminal.

12. The arrangement of claim 11 wherein: (i) a unidirectional voltage exists between the second transistor's common terminal and the first transistor's output terminal; and (ii) the absolute peak magnitude of the unidirectional voltage is larger than the absolute peak magnitude of the AC power line voltage.